REMARKS

Claims 1-9, 12, 17-20, and 22 are amended. A replacement drawing for FIG. 2 is provided, along with a mark-up version showing the changes made. No new matter is added; a "Prior Art" label is added.

Claims 10, 11, 13, and 17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,940,748 ("Nejad et al."). This rejection is respectfully traversed.

Claim 10 defines a memory integrated circuit and recites "a first two-dimensional array of resistive memory elements disposed in substantially parallel spaced relation between a second two-dimensional array of resistive memory elements and a third two-dimensional array of isolation devices, each isolation device of said third two-dimensional array being coupled to at least one resistive memory element of said first two-dimensional array and at least another resistive memory element of said second two-dimensional array." Claim 10 further recites "a first plurality of read/write conductors having respective longitudinal axes oriented in a first direction and coupled to said first two-dimensional array of resistive memory elements" and "a second plurality of read conductors having respective longitudinal axes also oriented in said first direction and also coupled to said first two-dimensional array of resistive memory elements." This structure is not disclosed by Nejad et al.

While it is true that there are some similarities between the memory structure of the claim and that of the reference, the Office Action (page 3) has pointed out a major difference between the structures. This difference is that the reference does not teach or suggest "a first plurality of read/write conductors having respective longitudinal axes oriented in a first direction and coupled to said first two-dimensional array of resistive

memory elements" and "a second plurality of read conductors having respective longitudinal axes also oriented in said first direction and also coupled to said first two-dimensional array of resistive memory elements." While the Office Action acknowledges that this difference exists, it thereafter attempts an explanation about why the reference could show a structure as defined in the claim, which is incorrect.

Without imposing any explanation or embodiment from the Specification into the claim limitations, a fair representation of the "axis" limitation(s) of this claim is illustrated by the embodiment shown in FIG. 1A (more so than FIGs. 4A or 4B, as suggested in the Office Action, which also fairly illustrate an embodiment of the recited subject matter). Claim 10 recites that the read/write conductors and read conductors of the claimed structure have "respective longitudinal axes" which are "oriented in a first direction." As shown by example in clearly in FIG. 1A (and also in FIGs. 4A and 4B), the longitudinal axes of these recited conductors are substantially parallel and the lengths of these conductors travel in substantially the same direction, i.e., the "first direction."

Contrary to the recited structure of the claim, Nejad et al. does not show analogous conductors having similar longitudinal axes orientations. In fact, the common read/write line (44) and the reading sense line (33) of Nejad et al. have axes shown to be and described as orthogonal to one another. Figures 1 and 2; col. 3, l. 64 to col. 4, l. 1. This orthogonal orientation provides for the memory cells (38) of Nejad et al. to be and defined at the intersection of the common line (44) and the sense line (33), which are oriented in tow different and opposing directions, i.e., not a first direction. The orthogonal relationship between the read lines of the reference's structure is the

opposite of the claimed structure, which positions analogous read lines parallel to one another in the same direction.

For the above reasons, independent claim 10 and dependent claims 11 and 13 are not anticipated by Nejad et al. Applicant respectfully requests that the 35 U.S.C. § 102(b) be withdrawn.

Claim 17, as amended, defines a magnetic random access memory device and recites, in part, "a first magnetic random access memory storage element over said upper surface and above said drain region and electrically coupled to said drain region through a first read conductor, said first read conductor having a first longitudinal axis" and "a second magnetic random access memory storage element over said upper surface and above said first magnetic random access memory storage element and electrically coupled to said first magnetic random access memory storage element and said drain region through a second read conductor, said second read conductor having a second longitudinal axis." Claim 17 also recites "first and second read/write conductors having respective third and fourth longitudinal axes, said first longitudinal axis being disposed substantially parallel to said third longitudinal axis, said second longitudinal axis being disposed substantially parallel to said fourth longitudinal axis." This is not taught or suggested by Nejad et al.

Similarly to claim 10, claim 17 includes that "said first read conductor having a first longitudinal axis" and "said second read conductor having a second longitudinal axis" and "first and second read/write conductors having respective third and fourth longitudinal axes, said first longitudinal axis being disposed substantially parallel to said third longitudinal axis, said second longitudinal axis being disposed substantially parallel to said fourth longitudinal axis." This claimed structure provides that the read

conductors have longitudinal axes that are parallel to the longitudinal axes of respective read/write conductors, i.e., they are in the same direction. As is the case with claim 10, Nejad et al. does not teach or suggest such a layout.

For the same reasoning as set forth above in relation to the patentability of claim 10 over Nejad et al., independent claim 17 is likewise not anticipated. Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of claim 17 be withdrawn.

Claims 1-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nejad et al. and U.S. Patent Application Publication No. 2005/0216244 ("Nahas"). This rejection is respectfully traversed.

Claim 1, as amended, defines a magnetic random access memory cell and recites "a first magnetic storage element having a first sense layer and a first pinned layer" and "a second magnetic storage element having a second sense layer and a second pinned layer, said first and second sense layers being mutually electrically coupled through first and second read conductors, said first and second read conductors having respective longitudinal axes, said first and second pinned layers being electrically coupled to respective first and second read/write conductors, said first and second read/write conductors having at least localized longitudinal axes in respective vicinities of said first and second magnetic storage elements, said at least localized longitudinal axes of said first read/write conductor being oriented substantially parallel to said longitudinal axis of said first read conductor." Claim 1 further includes "a switching device coupled to said mutually coupled pinned layers through said first and second read conductors and configured to couple said mutually coupled pinned layers to a conductor for receiving a substantially constant potential." Such a structure is not taught or suggested by Nejad et al. and Nahas.

The rejection of claim 1 relies on a misinterpretation of Nejad et al., as was so in the rejection of claims 10 and 17 addressed above. Nejad et al. does not teach or suggest "first and second read conductors having respective longitudinal axes" and "first and second read/write conductors having at least localized longitudinal axes" and "said at least localized longitudinal axes of said first read/write conductor being oriented substantially parallel to said longitudinal axis of said first read conductor." As discussed above, Nejad et al. discloses such conductors to have orthogonal longitudinal axes. Col. 3, l. 64 to col. 4, l. 1. Nahas does not remedy this lack of teaching or suggestion of Nejad et al. because the read conductor lines, i.e., 104 and 123/224 (no read/write lines are identified in the reference) of Nahas are also orthogonal to one another. For this reason, the claim is patentable over Nejad et al. and Nahas.

Additionally, the Office Action indicates (page 5) that it would have been obvious to connect the source of the switching device of Nejad et al. to ground, as such is well know per Nahas. This is incorrect. The access transistor (16) of Nejad et al. connects the memory cells to a sensing device, e.g., a sense amplifier (50). Therefore, if one were to instead make this connection to ground, as suggested in the Office Action, the devices of Nejad et al. would no longer function as intended; they would not be read. Nahas does not teach a way to otherwise connect the memory cells of Nejad et al. to the sense amplifiers (50) or otherwise remedy this. For this reason, too, the claim is patentable over the references.

Claim 4, as amended, defines a memory device and recites "a plurality of read/write conductors respectively paired with a plurality of read conductors, said respectively paired read/write and read conductors having substantially parallel longitudinal axes" and "at least one memory cell electrically coupled to each said

respectively paired read/write conductor and read conductor, said at least one memory cell including a transistor and two resistive memory elements, said two resistive memory elements being electrically connected in series by respective said read conductors, said two resistive memory elements being mutually coupled to said transistor at a common node." Such a device is not taught or suggested by Nejad et al. and Nahas.

As discussed above in relation to the patentability of independent claims 1 and 10, Nejad et al. and Nahas do not teach or suggest "a plurality of read/write conductors respectively paired with a plurality of read conductors, said respectively paired read/write and read conductors having substantially parallel longitudinal axes." The references disclose the opposite.

Independent claim 4 and dependent claims 5 and 6 are patentable over Nejad et al. and Nahas. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of these claims be withdrawn.

Claims 7-9, 12, 16, and 18-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nejad et al. in view of U.S. Patent 6,791,859 (Hush et al.). Applicant respectfully traverses this rejection.

Claims 7-9 depend from independent claim 4, which has been shown above to be patentable over Nejad et al. Hush et al. does not provide any teaching or suggestion to remedy the lack of disclosure of Nejad et al. with respect to the claimed subject matter. For example, Hush et al. does not teach or suggest "a plurality of read/write conductors respectively paired with a plurality of read conductors, said respective pairs of read/write and read conductors having substantially parallel

longitudinal axes," recited by claim 4. Therefore, for the same reasoning as set forth above for the patentability of claim 4, claims 7-9 are likewise patentable. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 7-9 over Nejad et al. and Hush et al. be withdrawn.

Claim 12 depends from independent claim 10, which has been discussed above as patentable over Nejad et al. Hush et al. fails to provide any teaching or suggestion to remedy the lack of disclosure of Nejad et al. with respect to the claimed subject matter. For example, Hush et al. does not teach or suggest "a first plurality of read/write conductors having respective longitudinal axes oriented in a first direction and coupled to said first two-dimensional array of resistive memory elements" and "a second plurality of read conductors having respective longitudinal axes also oriented in said first direction and also coupled to said first two-dimensional array of resistive memory elements," recited by claim 10. Therefore, for the same reasoning as set forth above for the patentability of claim 10, claim 12 is likewise patentable. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claim 12 over Nejad et al. and Hush et al. be withdrawn.

Claim 16 depends from independent claim 14, which is later rejected over Nejad et al., Hush et al. and Nahas. If independent 14 is unpatentable in the Examiner's view only over these three references combined, claim 16, which depends from claim 14, cannot be unpatentable over a lesser combination of references. For this reason, as well as for the reasons for patentability for claim 14 set forth below, Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claim 16 over Nejad et al. and Hush et al. be withdrawn.

Claim 18, as amended, defines a programmable conductive memory device and recites "a semiconductor substrate having an upper surface" and "a transistor having a drain region supported by said semiconductor substrate" and "a first programmable conductive memory storage element disposed above said upper surface and electrically coupled to said drain region by a first read conductor, said first read conductor having a first longitudinal axis" and "a second programmable conductive memory storage element disposed above said first programmable conductive memory storage element and electrically coupled to said first programmable conductive memory storage element and said drain region through a second read conductor, said second read conductor having a second longitudinal axis" and "first and second read/write conductors having respective third and fourth longitudinal axes, said first longitudinal axis being disposed substantially parallel to said third longitudinal axis, and said second longitudinal axis being disposed substantially parallel to said fourth longitudinal axis. " Such a device is not taught or suggested by Nejad et al. and Hush et al.

For the same reasoning as set forth above for the patentability of claims 7-9, 12, and 16 over Nejad et al. and Hush et al., independent claim 18 is likewise patentable. For example, the combined Nejad et al. and Hush et al. do not teach or suggest "said first read conductor having a first longitudinal axis" and "said second read conductor having a second longitudinal axis" and "first and second read/write conductors having respective third and fourth longitudinal axes, said first longitudinal axis being disposed substantially parallel to said third longitudinal axis, and said second longitudinal axis being disposed substantially parallel to said fourth longitudinal axis." As has been explained above, Nejad et al. discloses an opposite arrangement. Hush et al. cannot supplement Nejad et al. for such a disclosure.

For this reason, claim 18 is patentable over Nejad et al. and Hush et al. Applicant respectfully request that the 35 U.S.C. § 103(a) rejection of claim 18 be withdrawn.

Claim 19, as amended, defines a method of manufacturing a digital data storage device and recites "forming a transistor layer, including a plurality of transistors, over a semiconductor substrate" and "forming a first resistive memory storage layer over said transistor layer, said first resistive memory storage layer comprising a plurality of first resistive memory storage structures, each of said plurality of first resistive memory storage structures including respectively paired read conductors and read/write conductors, wherein said read conductors and said read/write conductors each have a respective longitudinal axis and said longitudinal axes of said respectively paired read conductors and read/write conductors are disposed in a substantially parallel relationship." Claim 19 further recites "forming a second magnetic memory storage layer over said first magnetic memory storage layer, said second magnetic memory storage layer comprising a plurality of second magnetic memory storage structures" and "electrically coupling respective ones of said plurality of transistors, said plurality of first magnetic memory storage structures, and said plurality of second magnetic memory storage structures." Such a method is not taught or suggested by Nejad et al. and Hush et al.

As discussed above in relation to other claims, neither Nejad et al. nor Hush et al. teaches or suggests "forming a first resistive memory storage layer over said transistor layer, said first resistive memory storage layer comprising a plurality of first resistive memory storage structures, each of said plurality of first resistive memory storage structures including respectively paired read conductors and read/write

conductors, wherein said read conductors and said read/write conductors each have a respective longitudinal axis and said longitudinal axes of said respectively paired read conductors and read/write conductors are disposed in a substantially parallel relationship." There is simply no substantially parallel relationship between any longitudinal axes of read and read/write conductive lines in the structures disclosed by the references.

For this reason, independent claim 19 and dependent claim 20 are patentable over Nejad et al. and Hush et al. Applicant respectfully request that the 35 U.S.C. § 103(a) rejection of claims 19 and 20 be withdrawn.

Claim 21 defines a processing system and recites "a plurality of memory cells, each cell including: first and second resistive memory storage elements, said first and second resistive memory storage elements being electrically coupled to respective first and second memory sensing circuits, said first and second resistive memory storage elements being mutually coupled to a reference potential through a wired-NOR FLASH memory style transistor." Such a system is not taught or suggested by Nejad et al. and Hush et al.

The Office Action is incorrect in its interpretation of Hush et al. (page 8). Hush et al. does not teach or suggest a "wired-NOR FLASH memory style transistor" coupled to memory cells. The two memory cells of Hush et al. (i.e., bits 102 and 106) are each connected to a single digit line (118) by respective single wordline gates (i.e. 105 and 107). This is not a configuration where two transistors are used for a single memory cell, as would a NOR-style configuration. For this reason, claim 21 is patentable over the references. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claim 21 be withdrawn.

Claim 22, as amended, defines a method of forming a memory device and recites, "forming a plurality of NOR FLASH-memory style transistors disposed in an array over a semiconductor substrate" and "forming an array of first resistive memory elements over said transistors" and "forming an array of second resistive memory elements over said first resistive memory elements" and "electrically coupling at least one second resistive memory element to a respective first resistive memory element and to a respective transistor."

As was discussed above in relation to claim 21, Nejad et al. and Hush et al. do not teach or suggest coupling any resistive memory element to "a plurality of NOR FLASH-memory style transistors disposed in an array over a semiconductor substrate." The transistor-memory cell relationship of both references is different from this claimed structure and no method of forming such a device is disclosed in either reference. For this reason, claim 22 is patentable over the references. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claim 22 be withdrawn.

Claims 14 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nejad et al. in view of Hush et al. and also Nahas. Applicant respectfully traverses this rejection.

Claim 14 defines a memory integrated circuit and recites "a plurality of memory cells, each cell including first and second resistive memory storage elements, said first and second resistive memory storage elements being electrically coupled to respective first and second memory sensing circuits, said first and second resistive memory storage elements being mutually coupled to a reference potential through a common dual transistor." Such a device is not taught or suggested by Nejad et al., Hush et al. and Nahas.

It is acknowledged in the Office Action that Hush et al. is relied upon for the dual transistor layout of this and other claims. As discussed above, each individual transistor of Hush et al. is configured to operate a single respective memory element, this is not a dual-transistor per memory element layout, as recited in the claim. For this reason, independent claim 14 and depending claims 15 and 16 are patentable over the references. Applicant respectfully request that the 35 U.S.C. § 103(a) rejection of claims 14 and 15 (and 16 as discussed above) be withdrawn.

In view of the above amendment, applicant believes the pending application is in condition for allowance. A notice of allowance for all pending claims is respectfully requested.

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Respectfully submitted,

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Attachments:
Appendix A (replacement drawings)

AMENDMENTS TO THE DRAWINGS

Attached hereto are replacement sheet(s) of drawings including changes to Figure 2.

Attachment: one (1) replacement sheet
one (1) mark-up sheet showing changes

APPENDIX A

Replacement Drawing for FIG. 2
(one mark-up sheet and one replacement sheet)

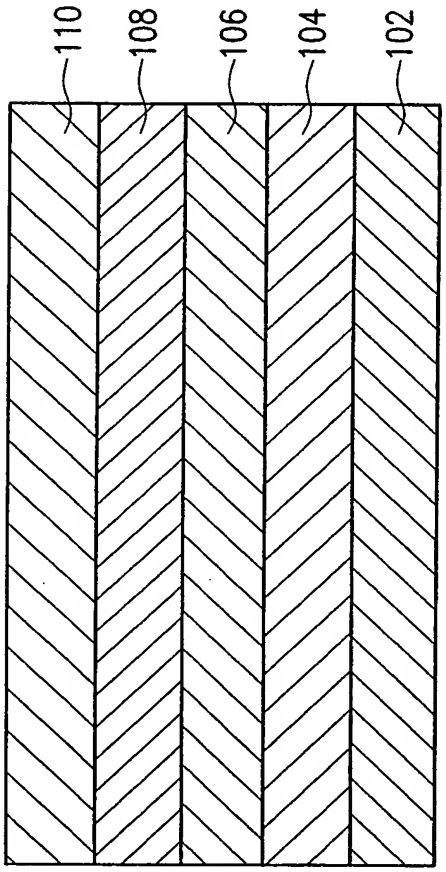

FIG. 2

PRIOR ART

MARK UP